DUPONT™

Supporting IC Substrate Development with Advanced Materials Technology

Packaging has become critical to chip technology, and the IC substrate market, which has become irreplaceable, is fundamentally determined by semiconductor package technology in terms of volume, technology, structure and value. The substrate industry thrived during the pandemic, as did the electronics industry overall, and it continues to grow. According to industry research firm Prismark, the IC substrate market reached US$10.2 billion in 2020, and is expected to reach 16.2 billion in 2025. Anticipated growth by supply chain segment is shown in Figure 1.

	2020/2019 Revenue Growth	2021F/2020 Revenue Growth	Comments and 2022 Outlook
OEM	2%	10%	2021 growth in all sectors, with supply chain concerns curbing higher growth. **2022 expect return to ~3% growth**
ODM/EMS	6%	12%	Limited impact from declining automotive/industrial/aerospace in 2020. **2022 >5% growth**
Semiconductor	7%	21%	Strong growth from all sectors and Increased semiconductor content. **2022 growth to continue at +8%**
PCB (Inc. Substrate)	6%	18%	PCB market benefit from packaging substrates, chip supply and pandemic recovery. **2022 growth of 5%**
Package Substrate	25%	27%	Growth buoyed by FCBGA demand and price increases **2022 growth of ~10%**

Figure 1. 2022 IC Substrate Supply Chain Growth Estimate (Source: Prismark)

Substrate Market Opportunities and Challenges

High integration and performance, miniaturization, and process development are key technological trends and challenges for IC substrates. New semiconductor and printed circuit board (PCB) technologies continually drive these requirements higher, especially the application of high-density connected manufacturing.

Digital evolution has brought changes and growth opportunities to electronic interconnects. High-performance computing (HPC) and artificial intelligence (AI) create higher functional requirements for electronic interconnection and require more I/O interfaces, which 5G and the Internet of Things drive RF-related technologies, which require higher efficiency, frequency and bandwidth. Also on the rise is heterogeneous integration – i.e., integration of 2.5D/3D and multiple electronic components into a single system in package (SiP). Achieving effective integration of various chip types and synergy between chips, package, systems and software is a major issue facing the industry.

One of the engines driving technological innovation is the miniaturization of mobile devices, which requires fine-line manufacturing for compliance with design requirements. Metallization of advanced

materials, application of dry film for fine-line circuits, and plating for uniformity all pose challenges to process development. In the application of dry film for fine-line circuits, miniaturization of devices requires smaller space with more electronic components, which will inevitably lead to fine-line circuits with finer width and space. At the same time, chip technology evolution leads to larger-sized IC substrates, higher integration of package units, and varied circuit designs. Internal forces between different material layers are likely to cause problems such as warpage, making it more challenging to achieve overall plating uniformity.

Materials Solutions to Substrate Challenges

DuPont Electronics & Industrial's materials solutions for IC substrates cover key technical areas in IC substrate manufacturing including desmear, electroless copper (Cu), electroplating Cu, dry film photoresist, advanced package build-up film, and photo-imageable dielectrics (see Figure 2). These offerings include advanced desmear for semi-additive processing (SAP), electroless copper, electroplating and filling, fine-line dry film, and advanced Cu pillar/bump photoresist and bumping.

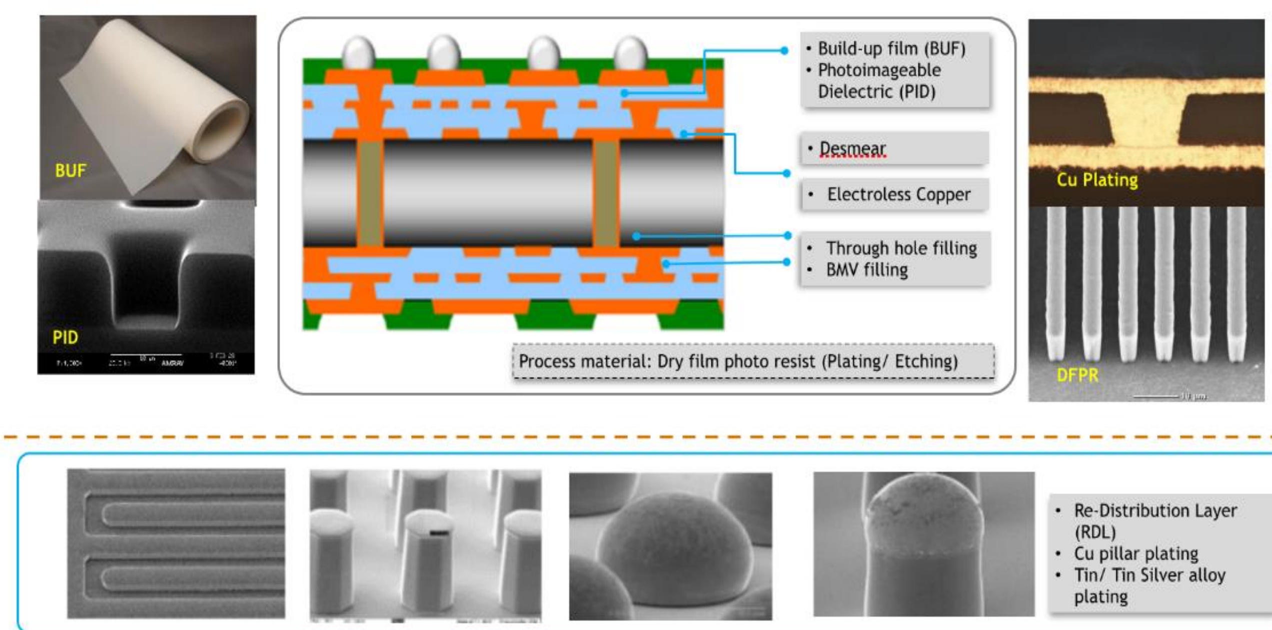

Figure 2. Key Processes in IC Substrate Manufacturing

DuPont Interconnect Solutions' offerings, shown in Figure 3, include copper-plating solutions for reliable IC packages and metallization compatible with customers' chosen dielectrics. Our surface treatments promote better adhesion, electroless Cu to accelerate deposition for the conductive dielectric layer, blind hole filling, copper pillars and redistribution layer (RDL) electroplating. Pure copper plating enables more reliable interconnect on IC substrates for ball grid arrays (BGAs) and chip scale packages (CSPs). With high throwing power for excellent thickness distribution and even coverage over IC substrates with complex geometry, DuPont metallization technology delivers ultra-high reliability to customers.

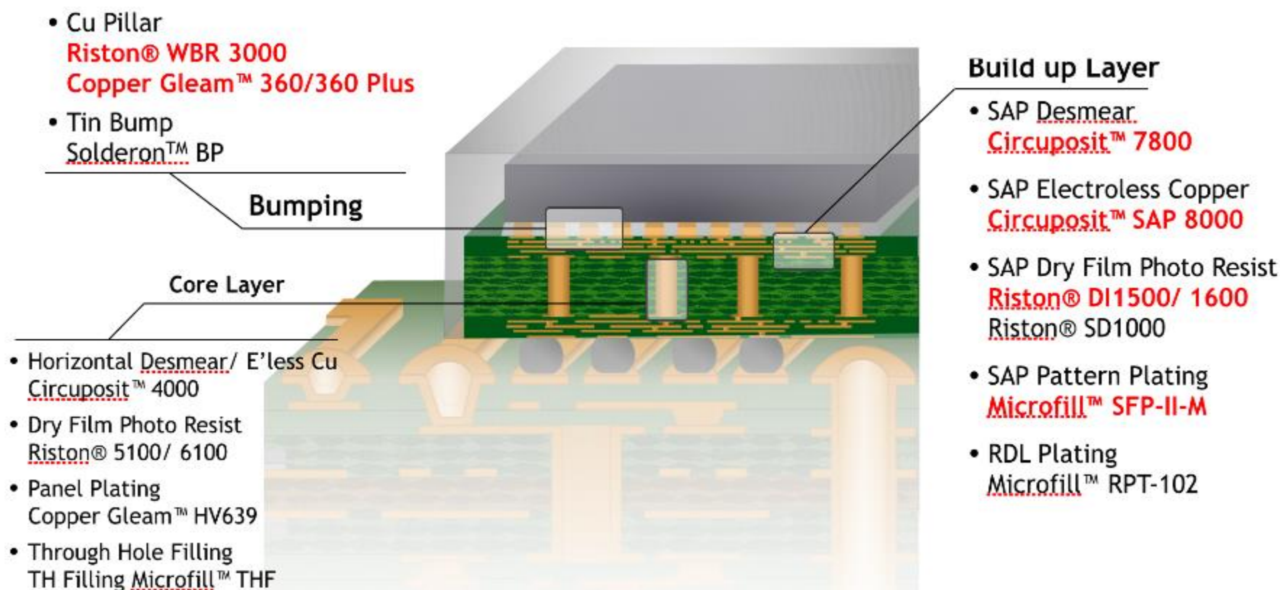

Figure 3. DuPont Interconnect Solutions Portfolio for IC Substrates

Our **Circuposit™ 7800** SAP desmear solution has uniform surface morphology on both conventional and advanced dielectrics, with excellent peeling strength and even performance. The desmear solution is used to deal with the smear residue left by the drilling of the multilayer board by preventing the smear from insulating the inner layer of copper and the hole copper. It also coarsens the hole wall to provide the resin surface with a good honeycomb-shaped surface roughness. This creates a better adhesion surface for the electroless Cu in subsequent production. Circuposit 7800's uniform surface morphology is conducive to subsequent metallization, especially the electroless copper deposition process, which brings excellent peeling strength and stable product quality.

Electroless copper plating deposits a Cu layer on the surface of the non-conductor (insulator) of the hole wall to ensure a reliable connection between the inner conductor and the circuit. **Circuposit™ SAP 8000**, our latest-generation SAP electroless Cu for IC substrates, features high throwing power plating and high peeling strength on advanced dielectrics. Its extraordinary Cu-Cu bonding force ensures excellent reliability performance.

Riston® DI1500/DI1600, our dry film solution for mSAP/SAP dry film photoresist processes, has strong chemical resistance to acidic cleaners before electroplating. Other key features include superior dot and fine-line adhesion and outstanding fine-line resolution.

For SAP pattern via-fill plating, DuPont provides **Microfill™ SFP-II-M**, with outstanding surface plating uniformity to support fine-line manufacturing for advanced IC substrates. It delivers good dimple and bump control to enable excellent via-filling performance. It also avoids plating void and skip plating, for outstanding yield and reliability. Adjusting parameters allows extension of this solution for use in through-hole filling applications, as well.

Finally, for Cu pillar processes, we offer two materials: **Riston® WBR3000**, our dry film solution for tall Cu pillar processes in advanced packaging applications, which has high aspect ratio, vertical pillar profile and wide photo latitude; and **Copper Gleam™ CP360/360 Plus**, our advanced solution for high-speed direct-current Cu pillar plating technology. **CP360/360 Plus** is widely used for different designs from 24 to 200 microns in height and delivers a wide range of plating current densities, up to 20 amps/decimeter^2 (ASD).

More details regarding our range of material offerings for IC substrate development and optimization can be found at https://www.dupont.com/electronic-materials/printed-circuit-boards.html.